Experimental Verification of MHz Inverter Constructed from Frequency Multiplying Circuit with Soft-Switching

Koji Orikawa, Nagaoka University of Technology, Japan, orikawa@vos.nagaokaut.ac.jp
Jun-ichi Itoh, Nagaoka University of Technology, Japan, itoh@vos.nagaokaut.ac.jp

Abstract

This paper discusses a verification of an inverter outputs MHz frequency without fast-switching semiconductor switches. The proposed inverter consists of a multi-phase inverter using silicon switching devices and multi-core transformers. By the frequency multiplying, the proposed circuit can output high frequency over the switching frequency. Moreover, the series resonance using a leakage inductance of the multi-core transformers and a resonant capacitor is applied in order to achieve sinusoidal output voltage. A prototype circuit is experimentally verified and theoretically analyzed in terms of soft-switching. As a result, it is confirmed the prototype circuit can output sinusoidal output voltage of 2.5 MHz with the switching frequency of 500 kHz. In addition, a required dead time for zero voltage switching is theoretically analyzed and experimentally verified using a prototype circuit.

1. Introduction

Recently, high-efficiency high-frequency inverters which output MHz frequency are increasingly received attentions for applications of wireless power transfer for EV chargers and plasma generators, and so on [1,2]. 6.78 MHz and 13.56 MHz are candidates for those applications as output frequency of the high-frequency inverters. On the other hand, wide gap semiconductors such as silicon carbide (SiC) and gallium nitride (GaN) are used widely due to fast-switching and low conduction loss. However, power consumption of a gate drive circuit becomes large in order to drive wide gap semiconductor [3]. In addition, it is difficult to control a gate signal of each switch due to low gate threshold voltage of SiC and GaN.

Class E inverters have been studying because they can achieve very high efficiency due to zero voltage switching (ZVS) and zero-derivative switching (ZDS) [4-7]. However, design of circuit parameters is difficult and it is designed by simulation. On the other hand, the inverter which can output high frequency over the switching frequency have been proposed by the authors [8]. In [8], the fundamental operation of the proposed circuit has been experimentally verified. In the proposed circuit, the switching frequency is lower than the output frequency. dv/dt of gate-source voltage is not high because semiconductor devices which have slow speed can be used. Therefore, the proposed circuit can supress EMI noise. However, the number of switch is large compared with that of conventional single phase inverter, the class E inverter, and so on. As a result, the switching loss at each phase of the multi-phase inverter should be reduced. In order to reduce the switching frequency, ZVS is effective. However, the condition which achieves ZVS in the proposed circuit has not been clarified so far.

This paper verifies experimentally the proposed circuit based on the frequency multiplying method using silicon switching devices and theoretically analyzed it in terms of the soft-switching. The proposed circuit can output frequency which is over switching frequency. First, the principle of the proposed circuit is described. Then, an operation of the proposed circuit is theoretically analyzed using an equivalent half-bridge circuit. Finally, a validity of the condition which achieves ZVS is experimentally verified at both cases without resonance and with resonance.

2. Proposed circuit based on frequency multiplying method

2.1. Circuit configuration

Figure 1 shows the circuit configuration of the proposed circuit in a five-phase inverter model. The primary side of the multi-core transformer [9] is connected in parallel. A common connection point of the primary side of the transformer is connected to the neutral point of DC link capacitors C_{dc}. On the other hand, the secondary side of the multi-core transformer is connected in series. The resonant capacitor which is used for the series resonance with the leakage inductance of the multi-core transformer is connected to the secondary side of the multi-core transformer. Note that magnetizing inductance is neglected.

Figure 2 shows the principle of the proposed frequency multiplying method. In the five phase voltage-type inverter, each of the voltage phases is shifted by 72 degree and operated with square wave modulation. As a result, the output frequency f_{out} is expressed by (1) using the switching frequency f_{sw} and the number of phase in the multi-phase inverter N.

$$f_{out} = N \times f_{sw} \qquad (1)$$

Therefore, the multi-phase inverter can output high frequency which is over the switching frequency even low switching frequency is used. If SiC switching devices are used in the proposed circuit, increasing of the output frequency and capacity of power converters is easy. In addition, cooling is easier because the heat generated from the multi-phase inverter can be dissipated for a number of switches.

2.2. Principle of zero voltage switching (ZVS)

Figure 3 describes the principle of ZVS in the proposed circuit for reduction of the switching loss. Fig. 3(a) shows a half bridge equivalent circuit of the proposed circuit. In Fig. 3(a), the DC link capacitor C_{dc} is assumed to be a voltage source. R is resistance components transformed to the primary side of the multi-core transformer, which includes a wire resistance r_1 and r_2 and a load resistance R_{load}. L is inductance components transformed to the primary side of the multi-core transformer, which includes a leakage inductance l_1 and l_2. C is an equivalent resonant capacitor. C_r is a resonant capacitor connected to the secondary side of the multi-core transformer. By analyzing the operation of the proposed circuit, R, L, C and C_r are expressed by (2), (3), (4) and (5) using turn ratio of the winding in the multi-core transformer n and the resonant frequency f_r.

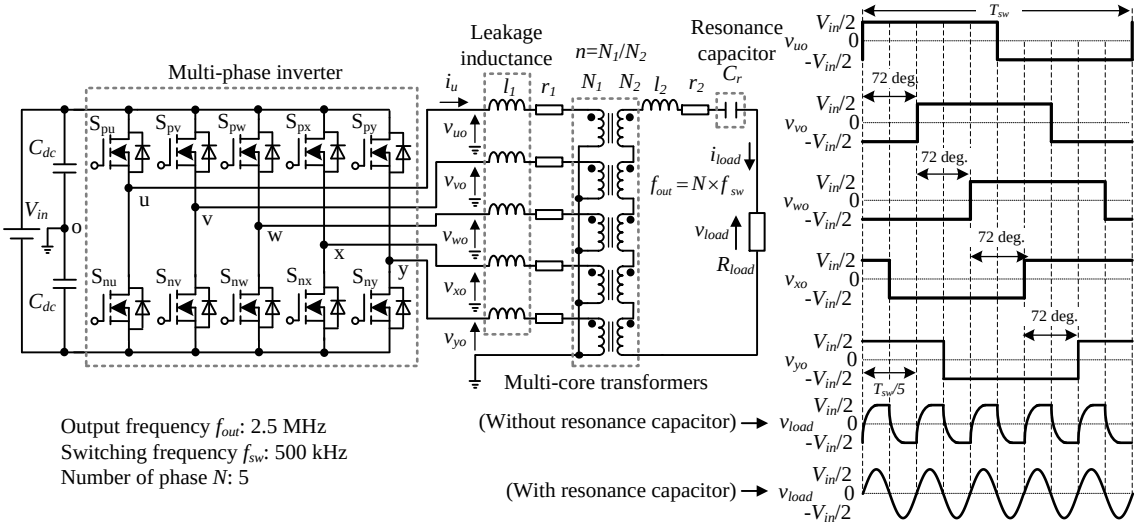
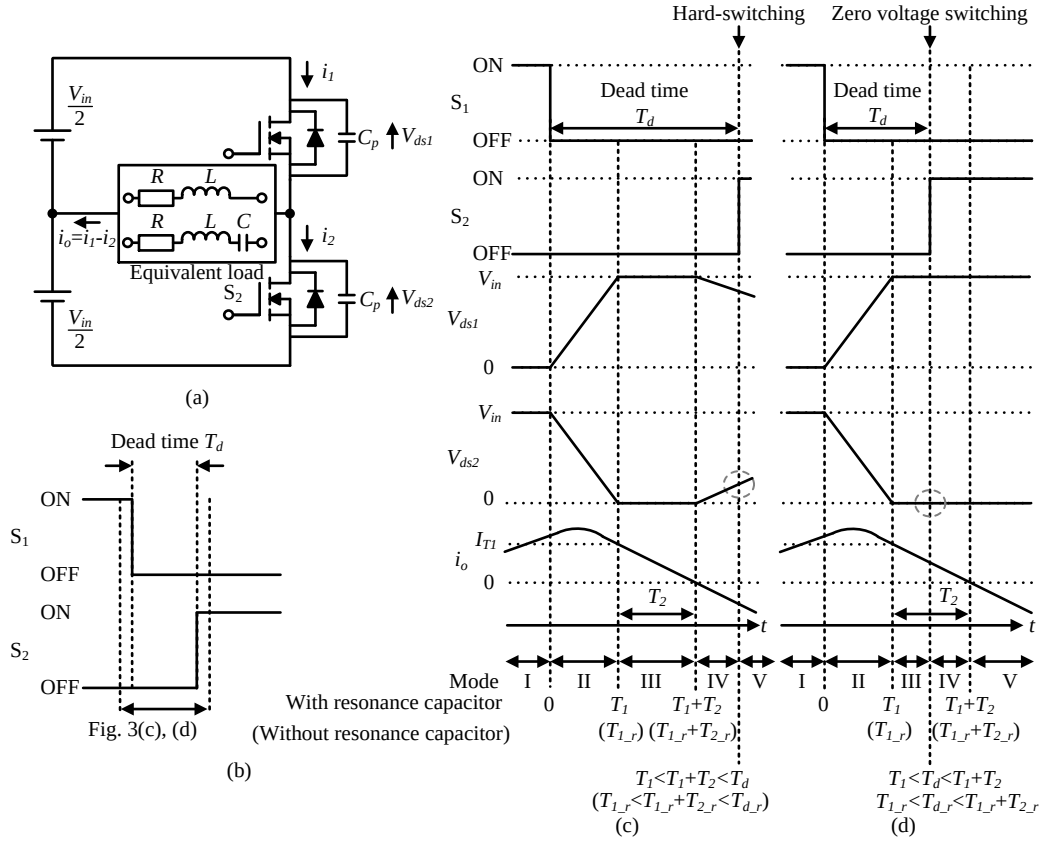


Fig. 1. Configuration of proposed circuit.

Fig. 2. Control method.

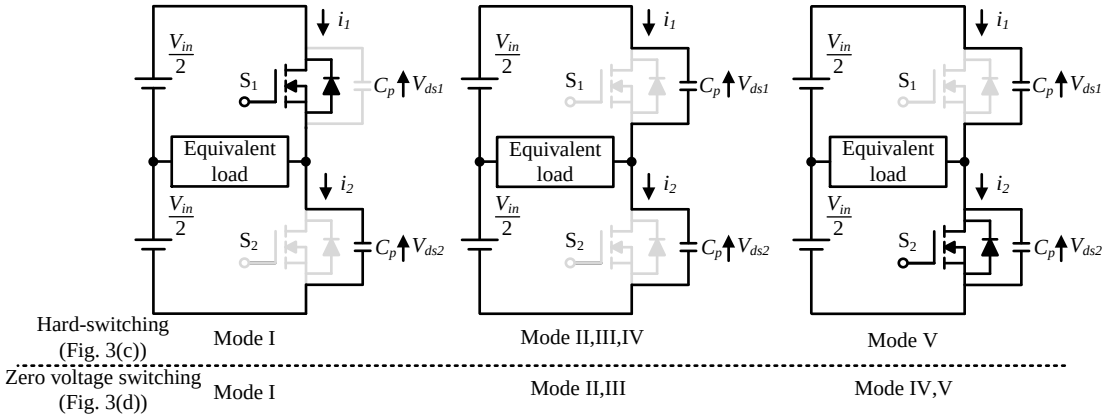
$$R = N \times r_1 + n^2 \times (R_{out} + r_2) \quad (2) \qquad L = N \times l_1 + n^2 \times l_2 \quad (3) \qquad C = 1/\{(2\pi f_r)^2 L\} \quad (4) \qquad C_r = n^2 C \quad (5)$$

Figure 4 shows operation mode of the proposed circuit. A condition which achieves ZVS is decided by the dead time and circuit parameters. In this section, the required dead time for ZVS in the proposed circuit at both cases without the resonant capacitor and with the



(a) Half bridge equivalent circuit. (b) Gate signals with dead-time.
(c) Enlarged waveforms at hard-switching.
(d) Enlarged waveforms at zero voltage switching.

Fig. 3. Principle of zero voltage switching.



(a) S_1:On, S_2:Off (b) S_1:Off, S_2:Off (c) S_1:Off, S_2:On

Fig. 4. Operation modes of the proposed circuit.

resonant capacitor is theoretically discussed by analyzing the operation modes of the equivalent circuit.

The case without the series resonance

i) Mode I

The Mode I is a period before the dead time starts. In the Mode I, the switch S_1 is on-state and the switch S_2 is off-state. Note that the current I_{Sw} flows to the S_1. In this paper, the period which the Mode I ends is defined as t=0.

ii) Mode II

In the Mode II, the S_1 is turned off and the period of the dead time starts. The Mode II is kept until the voltage of parasitic capacitance in S_1 is charged up to the input voltage or the voltage of the parasitic capacitance in S_2 is discharged to zero. Note that the period which the Mode II ends is defined as $t=T_1$. By solving the circuit equation of Fig. 3(a), the drain-source voltage of S_1 v_{ds1} is expressed by (6). Note that ω_1 is the natural angular frequency and K_1 is the coefficient. ω_1 and K_1 are expressed by (7) and (8).

$$v_{ds1}(t)=\frac{V_{in}}{2}\left\{1-\exp\left(-\frac{R}{2L}t\right)\left(\cos\omega_1 t+\frac{K_1}{\omega_1}\sin\omega t\right)\right\} \quad (6) \qquad \omega_1=\sqrt{\frac{1}{2LC_p}-\left(\frac{R}{2L}\right)^2} \quad (7) \qquad K_1=\frac{R}{2L}-\frac{I_{Sw}}{C_pV_{in}} \quad (8)$$

where V_{in} is the input voltage.

By solving (6) = 0, the T_1 which the Mode II ends is expressed by (9), provided that the circuit parameters satisfy (10).

$$T_1=\sqrt{2LC_p}\,Sin^{-1}\left\langle 4V_{in}/\left[\left\{\left(\frac{V_{in}}{\sqrt{\frac{L}{C_p}}}\right)^2\frac{1}{I_{sw}}+2I_{sw}\right\}\sqrt{2\frac{L}{C_p}}\right]\right\rangle \quad (9) \qquad C_pR<<2\frac{L}{R} \quad (10)$$

On the other hand, the current of the neutral point of the DC link voltage at $t=T_1$ is expressed by (11) using K_2, which is the coefficient value. K_2 is expressed by (12).

$$I_{T1}=i_1(T_1)-i_2(T_1)=I_{Sw}\exp\left(-\frac{R}{2L}T_1\right)\left(\cos\omega_1T_1+\frac{K_2}{\omega_1}\sin\omega_1T_1\right) \quad (11) \qquad K_2=\frac{V_{in}}{2LI_{Sw}}-\frac{R}{2L} \quad (12)$$

iii) Mode III

In the Mode III, $V_{in}/2$ is applied to the equivalent load of the equivalent circuit. Therefore, the current of the neutral point of the DC link voltage is expressed by (13). The time T_2 which the current polarity of the neutral point of the DC link voltage is changed is expressed by solving (13) = 0. From (13) = 0, T_2 is obtained by (14). If the dead time T_d is larger than T_1+T_2, the parasitic capacitance of drain-source in S_2 is charged. In this case, S_2 is turned on while the drain-source voltage of S_2 is not zero. Therefore, ZVS cannot be achieved. As a result, the required dead time which achieves ZVS T_d is expressed by (15) using T_1 and T_2.

$$i_o(t)=\left(I_{T1}-\frac{V_{in}}{2R}\right)e^{-\frac{R}{L}t}+\frac{V_{in}}{2R} \quad (13) \qquad T_2=\frac{L}{R}\ln\left(1-\frac{2RI_{T1}}{V_{in}}\right) \quad (14) \qquad T_1\le T_d\le T_1+T_2 \quad (15)$$

The case with the series resonance

i) Mode I

When the resonant capacitor is connected, the resonance occurs among the equivalent leakage inductance, the equivalent resonant capacitor and the parasitic capacitances of drain-source. Therefore, not only the current of S_1 I_{Sw1} but also the current of S_2 I_{Sw2} flows.

ii) Mode II

In the Mode II, v_{ds1} is expressed by (16)

$$v_{ds1}(t)=\frac{V_{in}}{2}\left\{1-\exp\left(-\frac{R}{2L}t\right)\left(\cos\omega_2 t+\frac{K_3}{\omega_2}\sin\omega_2 t\right)\right\} \quad (16)$$

where ω_2 is the natural angular frequency and K_3 is the coefficient. ω_2 and K_3 are expressed by (17) and (18).

$$\omega_2=\sqrt{\frac{1}{2LC_p}\left(1+\frac{2C_p}{C}\right)-\left(\frac{R}{2L}\right)^2} \quad (17) \qquad K_3=\frac{R}{2L}-\frac{I_{Sw1}-I_{Sw2}}{C_pV_{in}} \quad (18)$$

From (16) = 0, T_{1_r} which the Mode II ends can be obtained. However, T_{1_r} is almost same to T_1, provided that (7) is assumed to be satisfied.

On the other hand, the current of the neutral point of the DC link voltage at $t=T_{1\_r}$ is expressed by (19) using K_4, which is the coefficient value. K_4 is expressed by (20).

$$\begin{aligned} I_{T1} &= i_1(T_1)-i_2(T_1) \\ &= (I_{Sw1}-I_{Sw2})\exp\left(-\frac{R}{2L}T_1\right)\left(\cos\omega_2 T_1+\frac{K_4}{\omega_2}\sin\omega_2 T_1\right) \end{aligned} \quad (19)$$

$$K_4=\frac{V_{in}}{2L(I_{Sw1}-I_{Sw2})}\left(1+\frac{2C_p}{C}\right)-\frac{R}{2L} \quad (20)$$

iii) Mode III

In the Mode III, $V_{in}/2$ is applied to the equivalent load of the equivalent circuit. Therefore, the current of the neutral point of the DC link voltage is expressed by (21) by solving the transient phenomenon of the equivalent circuit. Note that ω_3 is the natural angular frequency and K_5 is the coefficient. ω_3 and K_5 are expressed by (22) and (23).

$$i_o=I_{T1}\exp\left(-\frac{R}{2L}t\right)\left(\cos\omega_3 t+\frac{K_5}{\omega_3}\sin\omega_3 t\right) \quad (21) \qquad \omega_3=\sqrt{\frac{1}{2LC}-\left(\frac{R}{2L}\right)^2} \quad (22) \qquad K_5=\frac{\frac{V_{in}}{2}-V_c(0)}{LI_{T1}}-\frac{R}{2L} \quad (23)$$

where $V_c(0)$ is the voltage of the equivalent resonant capacitor at $t=T_{1\_r}$.

The time T_{2_r} which the current polarity of the neutral point of the DC link voltage is changed in the Mode III is obtained by (24) from (21) = 0. As a result, the required dead time T_{d_r} which achieves ZVS when the resonant capacitor is connected is expressed by (25) using T_1 and T_{2_r}.

$$\cos\omega_3 T_2+\frac{K_5}{\omega_3}\sin\omega_3 T_2=0 \quad (24) \qquad T_1\le T_{d\_r}\le T_1+T_{2\_r} \quad (25)$$

3. Experimental results

3.1. The case without the series resonance

Figure 5 shows fundamental waveforms without the series resonant capacitor. In Fig. 5, the dead time which satisfies (15) is used. The switching frequency and the output frequency is 500 kHz and 2.5 MHz. A resistance of 33.3 Ω is connected as a load. The input voltage V_{in} is 48 V. From Fig. 5, it is confirmed that v_{load} is not a square waveform because the impedance of leakage inductances is large at the output frequency of 2.5 MHz.

Figure 6 and 7 show experimental waveforms which include two gate signals, the drain-source voltage of S_2 and the primary current of the multi-core transformer. In these

experiments, the dead time is changed. In Fig. 6(a) and Fig. 7(a), the dead time which satisfies (15) is used. In Fig. 7(a), after the polarity of the output current in U-phase i_u is changed, v_{gs2} is turned on rapidly. Therefore, the parasitic capacitance drain-source in the S_2 is not charged. As a result, ZVS is achieved because v_{ds2} is zero when v_{gs2} is turned on.

On the other hand, in Fig. 7(b) and (c), the used dead time does not satisfy (15). v_{ds2} has a resonance between the leakage inductance and the parasitic capacitances of

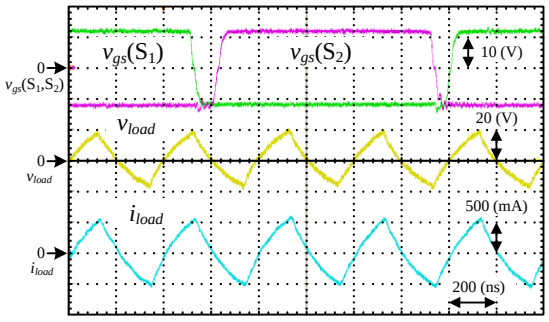


Fig. 5. Fundamental waveforms without resonance capacitor (T_1<T_d<T_1+T_2, T_d=112.7 ns).

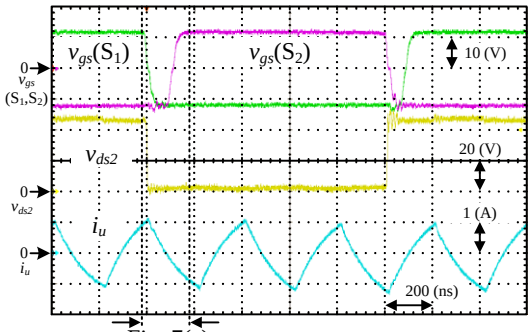
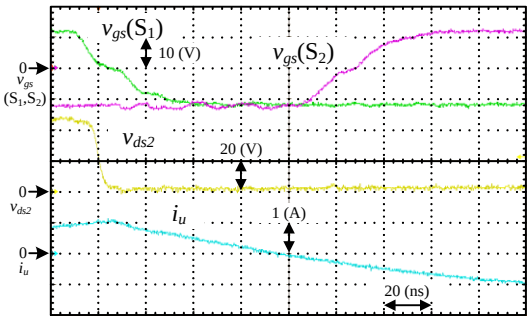


Fig. 7(a)

(a) T_1<T_d<T_1+T_2 (T_d=112.7 ns).



(a) T_1<T_d<T_1+T_2 (T_{d_r}=112.7 ns).

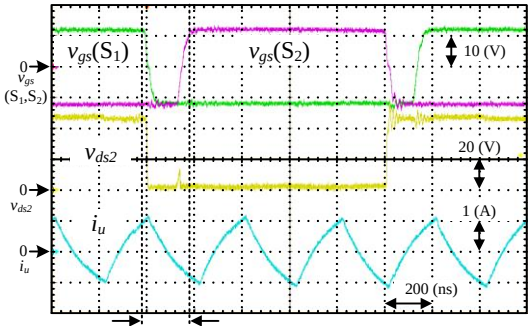
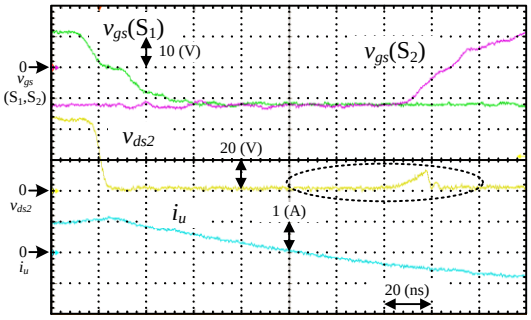


Fig. 7(b)

(b) T_1<T_1+T_2<T_d (T_d=151.2 ns).



(b) T_1<T_1+T_2<T_d (T_d=151.2 ns).

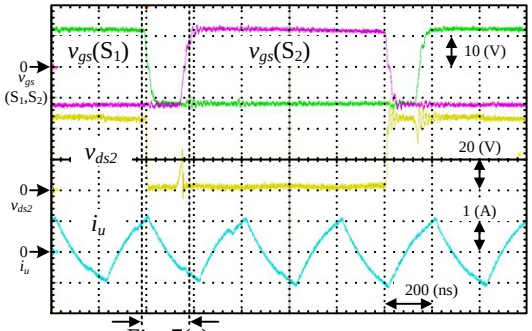
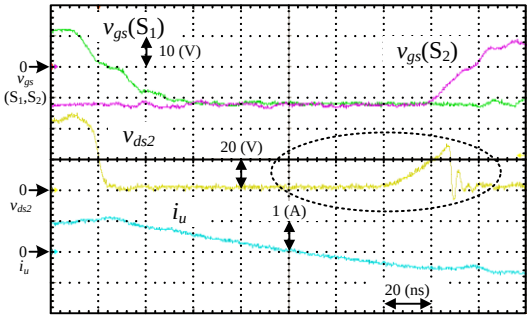


Fig. 7(c)

(c) T_1<T_1+T_2<T_d (T_d=160.6 ns).

Fig. 6. Whole waveforms without series resonance.



(c) T_1<T_1+T_2<T_d (T_d=160.6 ns).

Fig. 7. Enlarged waveforms of Fig. 6.

drain-source during the dead time. Therefore, in Fig. 7(b) and (c), ZVS is not achieved when v_{gs2} is turned on. From Fig. 7, the validity of the theoretical discussion in the chapter II was experimentally confirmed.

3.2. The case with the series resonance

Figure 8 shows the fundamental waveforms when the series resonance is applied. The resonance capacitor is connected to the secondary side of the multi-core transformers. In Fig. 8, the dead

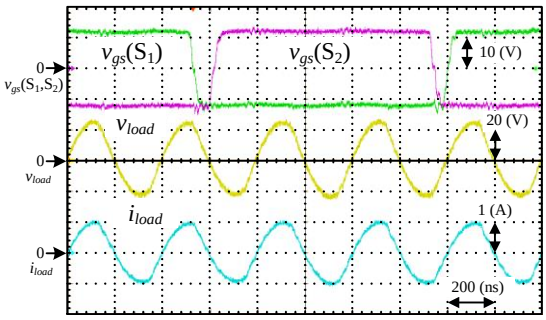


Fig. 8. Fundamental waveforms with resonant capacitor (T_1<T_{d_r}<T_{1_r}+T_{2_r},T_{d_r}=98.5 ns).

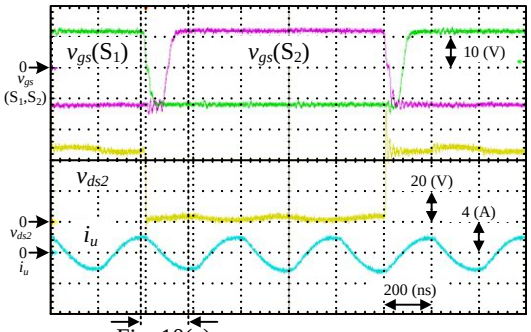
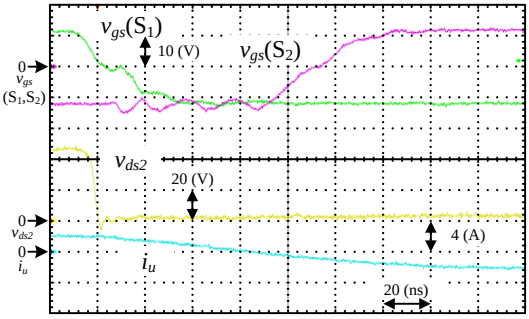


Fig. 10(a)

(a) T_1<T_{d_r}<T_{1_r}+T_{2_r} (T_{d_r}=98.5 ns).



(a) T_1<T_{d_r}<T_{1_r}+T_{2_r} (T_{d_r}=98.5 ns).

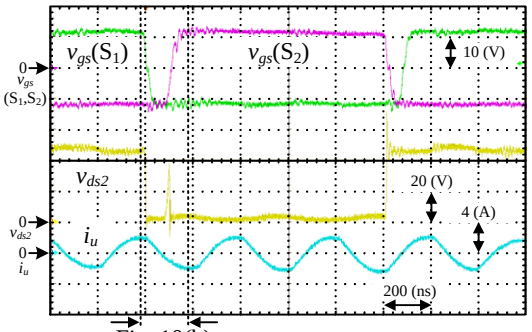
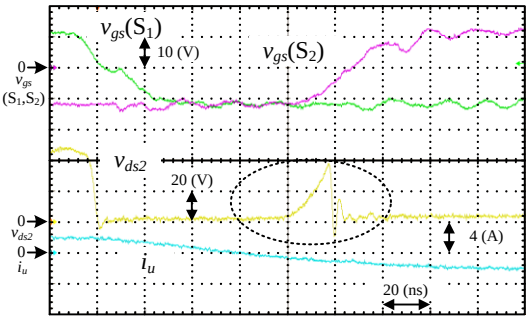


Fig. 10(b)

(b) T_1<T_{1_r}+T_{2_r}<T_{d_r} (T_{d_r}=109.7 ns).



(b) T_1<T_{1_r}+T_{2_r}<T_{d_r} (T_{d_r}=109.7 ns).

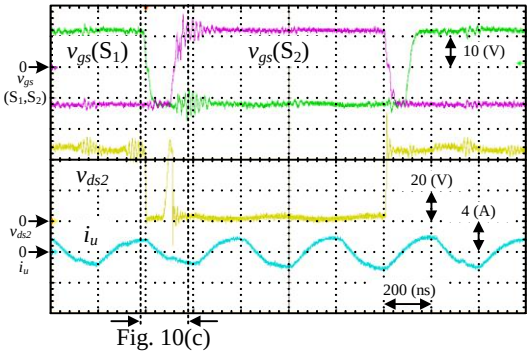
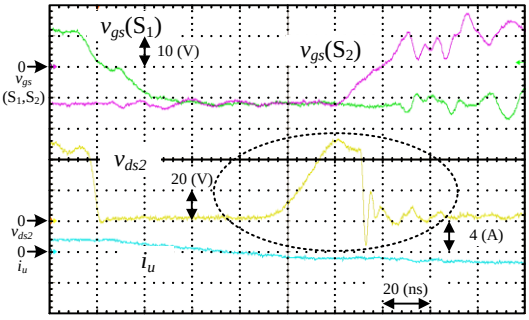


Fig. 10(c)

(c) T_1<T_{1_r}+T_{2_r}<T_{d_r} (T_{d_r}=123.7 ns).

Fig. 9. Whole waveforms with series resonance.



(c) T_1<T_{1_r}+T_{2_r}<T_{d_r} (T_{d_r}=123.7 ns).

Fig. 10. Enlarged waveforms of Fig. 9.

time which satisfies (25) is used. From Fig. 8, it is confirmed that the load voltage is almost sinusoidal waveform due to the series resonance.

Figure 9 and 10 show experimental waveforms which include two gate signals, the drain-source voltage of S_2 and the primary current of the multi-core transformer when the resonant capacitor is connected. In Fig. 9(a) and Fig. 10(a), there is no rise of v_{ds2} during the dead time because the dead time which satisfies (25) is used. Therefore, not only when the series resonance is not applied but also when the series resonance is applied, ZVS is achieved. Therefore, the sinusoidal output at soft-switching on the proposed circuit is achieved. On the other hand, in Fig. 10(b) and (c), the used dead time does not satisfy (25). Therefore, hard-switching occurs because v_{ds2} is increased during the dead time. From these experiments, the proposed circuit can obtain high efficiency even the output frequency is 2.5MHz.

4. Conclusion

This paper describes the high-frequency inverter outputs MHz frequency without fast-switching devices. By the frequency muliplying, the proposed circuit can output high frequency over the switching frequency. First, the required dead time which achieves ZVS was calculted by using the equivalent circuit. Finally, the protoype circuit was experimentally verified. It was confirmed the prototype circuit can output 2.5 MHz with the switching frequency of 500 kHz at ZVS condition. In addition, it was experimentally confirmed that only when the series resonance is not applied but also when the series resonance is applied, ZVS is achieved.

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